

IN THE CLAIMS:

Please substitute the following claims for the same-numbered claims in the application:

1-7. (Cancelled).

8. (Currently Amended) A field effect transistor comprising:

a silicon substrate,

wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and

wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth;

an epitaxial silicon halo layer on said top surface of said silicon substrate;

an epitaxial silicon source/drain layer on said epitaxial silicon halo layer; and

a gate stack above said epitaxial silicon source/drain layer.

9. (Original) The field effect transistor in claim 8, wherein source/drain dopants are substantially limited to said epitaxial silicon source/drain layer.

10. (Currently Amended) The field effect transistor in claim 8, wherein said increased oxygen content substantially limits dopants within said epitaxial silicon halo layer and said eptiaxial silicon source/drain layer from moving into said silicon substrate.

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11. (Currently Amended) The field effect transistor in claim 8, wherein said silicon substrate includes a column portion extending through said epitaxial silicon ~~panel~~ halo layer and said epitaxial silicon source/drain layer, wherein said column portion is below said gate stack ~~conductor~~.

12. (Currently Amended) The field effect transistor in claim ~~[[8]]~~ 9, wherein halo dopants are substantially limited to said epitaxial silicon halo layer and wherein said halo dopants are different from said source/drain dopants.

13. (Original) The field effect transistor in claim 8, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

14. (Currently Amended) The field effect transistor in claim 8, wherein said top surface is essentially damage and native oxide free ~~further comprising sidewall spacers on said gate~~ ~~conductor~~.

15-34. (Cancelled).

35. (New) A field effect transistor comprising:
a silicon substrate,

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wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and

wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth from said silicon substrate; and

an epitaxial silicon layer directly on said top surface of said silicon substrate, grown from said silicon substrate and comprising dopants,

wherein said dopants are substantially limited to said epitaxial silicon layer by said increased oxygen content of said top surface of said silicon substrate.

36. (New) The field effect transistor in claim 35, wherein said dopants comprise source/drain dopants and halo dopants and wherein said source/drain dopants and said halo dopants are different.

37. (New) The field effect transistor in claim 35, wherein said increased oxygen content limits said dopants within said epitaxial silicon layer from moving into said silicon substrate.

38. (New) The field effect transistor in claim 35, wherein said epitaxial silicon layer comprises an in-situ doped epitaxial silicon layer.

39. (New) The field effect transistor in claim 35, further comprising source/drain regions in said epitaxial silicon layer.

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40. (New) The field effect transistor in claim 35, further comprising isolation regions in said epitaxial silicon layer and said silicon substrate.

41. (New) The field effect transistor in claim 35, wherein said top surface is essentially damage and native oxide free.

42. (New) A field effect transistor comprising:

a silicon substrate,

wherein the top surface of said silicon substrate has an increased oxygen content when compared to other portions of said silicon substrate, and

wherein said oxygen content of said top surface of said silicon substrate is below an amount that would prevent epitaxial growth from said silicon substrate;

an epitaxial silicon source/drain layer directly on said top surface of said silicon substrate, grown from said silicon substrate and comprising source/drain dopants,

wherein said source/drain dopants are substantially limited to said epitaxial silicon source/drain layer by said increased oxygen content of said top surface of said silicon substrate.

43. (New) The field effect transistor in claim 42, wherein said increased oxygen content substantially limits said source/drain dopants within said epitaxial silicon source/drain layer from moving into said silicon substrate.

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44. (New) The field effect transistor in claim 42, wherein said silicon substrate includes a column portion extending through said epitaxial silicon source/drain layer, wherein said column portion is below said gate stack.
45. (New) The field effect transistor in claim 42, wherein said top surface is essentially damage and native oxide free.
46. (New) The field effect transistor in claim 42, wherein said epitaxial silicon source/drain layer comprises an in-situ doped epitaxial silicon source/drain layer.
47. (New) The field effect transistor in claim 42, further comprising isolation regions in said epitaxial silicon source/drain layer and said silicon substrate.

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